IN THE CLAIMS

Listing of Claims:

1. (original) A receiver circuit for terminating a transmission line comprising:

a receiver having an input coupled to a transmission line output of said transmission line forming a common node, an output generating a digital signal in response to a signal at said transmission line output and a threshold voltage;

a termination network coupled to said common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals; and

logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs.

2. (previously presented) A receiver circuit for terminating a transmission line comprising:

a receiver having an input coupled to a transmission line output of said transmission line forming a common node, an output generating a digital signal in response to a signal at said transmission line output and a threshold voltage;

a termination network coupled to said common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals; and

logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs, wherein said termination network comprises a first termination network coupled to said common node and setting a Thevenins impedance and a Thevenins voltage at said common node and a second termination network coupled to said common node and modifying said Thevenins impedance an said Thevenins voltage in response to first and second control signals.

3. (original) The circuit of claim 2 further comprising a third termination network coupled to said common node and modifying said Thevenins impedance and said

Thevenins voltage in response to third and fourth control signals generated by said logic circuitry.

4. (original) The circuit of claim 2, wherein said first termination network is coupled to said common node in response to fifth and sixth control signals generated by said logic circuitry.

5. (currently amended) The circuit of claim 4, wherein said second ~~first~~ termination network comprises:

a first resistor having a first terminal coupled to a first power supply voltage with a first electronic switch in response to a first logic state of said first control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to a second power supply voltage with a second electronic switch in response to a first logic state of said second control signal.

6. (currently amended) The circuit of claim [[2]]3, wherein said third ~~second~~ termination network comprises:

a first resistor having a first terminal coupled to said first power supply voltage with a first electronic switch in response to a first logic state of said third control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to a second power supply voltage with a second electronic switch in response to a first logic state of said fourth control signal.

7. (currently amended) The circuit of claim [[3]]4, wherein said first ~~third~~ termination network comprises:

a first resistor having a first terminal coupled to said first power supply voltage with a first electronic switch in response to a first logic state of said fifth control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to said second power supply voltage with a second electronic switch in response to a first logic state of said sixth control signal.

8. (original) The circuit of claim 2, wherein said receiver circuit is a logic gate having a first logic input coupled to said receiver input, a second logic input coupled to a voltage corresponding to a first logic state, wherein said threshold voltage is a switching voltage of said logic gate and is generated internal to said logic gate.

9. (original) The circuit of claim 2, wherein said receiver circuit is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output.

10. (original) The circuit of claim 4, wherein said receiver circuit is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output.

11. (original) The circuit of claim 7, wherein said threshold voltage is equal to one half the difference between said first and second power supply voltages.

12. (currently amended) The circuit of claim 4, wherein said mode inputs comprise a first mode input for setting said Thevenins impedance to substantially match a characteristic impedance of said ~~TL~~ transmission line (TL) and said Thevenins voltage to

substantially match said threshold voltage, wherein said first, second, ~~fourth and~~ fifth and sixth electronic switches are gated ON by said first , second , ~~fourth and~~ fifth and sixth control signals.

13. (original) The circuit of claim 12, wherein said mode inputs comprise a second mode for setting said Thevenins impedance to substantially match a characteristic impedance of said TL and said Thevenins voltage to greater than said threshold voltage, wherein said first, second, third and fifth electronic switches are gated ON by said first, second, third and fifth control signals.

14. (original) The circuit of claim 13, wherein said mode inputs comprise a third mode for setting said Thevenins impedance to substantially match a characteristic impedance of said TL and said Thevenins voltage to less than said threshold voltage, wherein said first, second fourth and sixth electronic switches are gated ON by said first, second fourth and sixth control signals.

15. (original) The circuit of claim 14, wherein said mode inputs comprise a fourth mode for setting said Thevenins impedance to greater than a characteristic impedance of said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein said first and second electronic switches are gated on by said first and second control signals.

16. (original) The circuit of claim 15, wherein said mode inputs comprise a fifth mode for setting said Thevenins impedance to less than a characteristic impedance of said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein said first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said first, second, third, fourth, fifth, and sixth control signals.

17. (original) The circuit of claim 16, wherein said mode inputs comprise a driver mode wherein said first, second, and third termination networks operate as a driver

circuit for impressing a drive signal on said common node in response to logic states of a driver signal controlling said first, second, third, fourth, fifth and sixth control signals, wherein said second, fourth and sixth electronic switches are gated ON by a first logic state of said driver signal and said first, third, and fifth electronic switches are gated ON by a second logic state of said driver signal.

18. (original) The circuit of claim 15, wherein said logic circuitry comprises:

circuitry for alternating between selected of said first, second, third, fourth, and fifth modes in response to a first logic state of a dynamic enable signal and logic states of a modified receiver output signal;

a state circuit for generating said modified receiver signal in response to said receiver output signal and a selected delay time .

19. (original) The circuit of claim 18, wherein said modified receiver transitions to a first logic state said delay time after said receiver output signal transitions to said first logic state and to a second logic state said selected delay time after said receiver signal transitions to said second logic state, wherein said selected delay time is set by delay control signal.

20. (original) The circuit of claim 19, wherein said circuitry switches to said fourth mode when said modified receiver signal has a first logic state and switches to said fifth mode when said modified receiver signal has a second logic state.

21. (original) The circuit of claim 18, wherein said first logic state of said dynamic mode signal is set in response to a selected signal quality parameter of said receiver output signal.

22. (original) An integrated circuit (IC) comprising:

a digital processor;

memory for storing instructions and data for said processor;

input/output (I/O) interface circuitry for communicating to device circuitry external to said IC;

a receiver circuit in said interface circuitry for terminating a transmission line coupling said receiver circuit to said device circuitry, said receiver circuit further comprising;

a receiver having an input coupled to a transmission line output of said transmission line forming a common node, an output generating a digital signal in response to a signal at said transmission line output and a threshold voltage;

a termination network coupled to said common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals; and

logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs.

23. (previously presented) An integrated circuit (IC) comprising:

a digital processor;

memory for storing instructions and data for said processor;

input/output (I/O) interface circuitry for communicating to device circuitry external to said IC;

a receiver circuit in said interface circuitry for terminating a transmission line coupling said receiver circuit to said device circuitry, said receiver circuit further comprising;

a receiver having an input coupled to a transmission line output of said transmission line forming a common node, an output generating a digital signal in response to a signal at said transmission line output and a threshold voltage;

a termination network coupled to said common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals; and

logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs, wherein said termination network comprises a first termination network coupled to said common node for setting a Thevenins impedance and a Thevenins voltage at said common node and a second termination network coupled to said common node for modifying said Thevenins impedance and said Thevenins voltage in response to first and second control signals.

24. (original) The IC of claim 23 further comprising a third termination network coupled to said common node and modifying said Thevenins impedance and said Thevenins voltage in response to third and fourth control signals generated by said logic circuitry.

25. (original) The IC of claim 23, wherein said first termination network is coupled to said common node in response to fifth and sixth control signals generated by said logic circuitry.

26. (currently amended) The IC of claim 25, wherein said second ~~first~~ termination network comprises:

a first resistor having a first terminal coupled to a first power supply voltage with a first electronic switch in response to a first logic state of said first control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to a second power supply voltage with a second electronic switch in response to a first logic state of said second control signal.

27. (currently amended) The IC of claim [[23]]24, wherein said third ~~second~~ termination network comprises:

a first resistor having a first terminal coupled to said first power supply voltage with a first electronic switch in response to a first logic state of said third control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to a second power supply voltage with a second electronic switch in response to a first logic state of said fourth control signal.

28. (currently amended) The IC of claim [[24]]25, wherein said first ~~third~~ termination network comprises:

a first resistor having a first terminal coupled to said first power supply voltage with a first electronic switch in response to a first logic state of said fifth control signal and a second terminal;

a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to said second power supply voltage with a second electronic switch in response to a first logic state of said sixth control signal.

29. (original) The IC of claim 23, wherein said receiver circuit is a logic gate having a first logic input coupled to said receiver input, a second logic input coupled to a voltage corresponding to a first logic state, wherein said threshold voltage is a switching voltage of said logic gate and is generated internal to said logic gate.

30. (original) The IC of claim 23, wherein said receiver circuit is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output.

31. (original) The IC of claim 25, wherein said receiver circuit is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output.

32. (original) The IC of claim 28, wherein said threshold voltage is equal to one half the difference between said first and second power supply voltages.

33. (currently amended) The IC of claim 25, wherein said mode inputs comprise a first mode input for setting said Thevenins impedance to substantially match a characteristic impedance of said ~~TL~~ transmission line (TL) and said Thevenins voltage to substantially match said threshold voltage, wherein said first, second, fourth and fifth electronic switches are gated ON by said first , second , fourth and fifth control signals.

34. (original) The IC of claim 33, wherein said mode inputs comprise a second mode for setting said Thevenins impedance to substantially match a characteristic impedance of said TL and said Thevenins voltage to greater than said threshold voltage, wherein said first, second, third and fifth electronic switches are gated ON by said first, second, third and fifth control signals.

35. (original) The IC of claim 34, wherein said mode inputs comprise a third mode for setting said Thevenins impedance to substantially match a characteristic impedance of said TL and said Thevenins voltage to less than said threshold voltage, wherein said first, second fourth and sixth electronic switches are gated ON by said first, second fourth and sixth control signals.

36. (original) The IC of claim 35, wherein said mode inputs comprise a fourth mode for setting said Thevenins impedance to greater than a characteristic impedance of said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein said first and second electronic switches are gated on by said first and second control signals.

37. (original) The IC of claim 36, wherein said mode inputs comprise a fifth mode for setting said Thevenins impedance to less than a characteristic impedance of said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein said first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said first, second, third, fourth, fifth, and sixth control signals.

38. (original) The IC of claim 37, wherein said mode inputs comprise a driver mode wherein said first, second, and third termination networks operate as a driver circuit for impressing a drive signal on said common node in response to logic states of a driver signal controlling said first, second, third, fourth, fifth and sixth control signals, wherein said second, fourth and sixth electronic switches are gated ON by a first logic state of said driver signal and said first, third, and fifth electronic switches are gated ON by a second logic state of said driver signal.

39. (original) The IC of claim 36, wherein said logic circuitry comprises:

circuitry for alternating between selected of said first, second, third, fourth, and fifth modes in response to a first logic state of a dynamic enable signal and logic states of a modified receiver output signal;

a state circuit for generating said modified receiver signal in response to said receiver output signal and a selected delay time .

40. (original) The IC of claim 39, wherein said modified receiver transitions to a first logic state said delay time after said receiver output signal transitions to said first logic state and to a second logic state said selected delay time after said receiver signal transitions to said second logic state, wherein said selected delay time is set by delay control signal.

41. (original) The IC of claim 40, wherein said circuitry switches to said fourth mode when said modified receiver signal has a first logic state and switches to said fifth mode when said modified receiver signal has a second logic state.

42. (original) The IC of claim 39, wherein said first logic state of said dynamic mode signal is set in response to a selected signal quality parameter of said receiver output signal.